Simulation and Analysis of GaN CMOS Logic

J. Jung, N. Chowdhury, Q. Xie, and T. Palacios

Sponsorship: MIT EECS - Texas Instruments Undergraduate Research and Innovation Scholar

There is an increasing demand for electronics that can operate in high-temperature conditions, such as spacecraft and sensors for industrial environments. Electronics based on wide-bandgap materials offer a promising solution, among which gallium nitride (GaN) stands out as a strong candidate due to its excellent material properties and potential for monolithic integration. Most current demonstrations of GaN logic are based on nMOS technology, which has a high static power consumption. GaN CMOS technology, which has lower static power consumption, is desired.

This work studies the effect of p-channel transistor performance and circuit parameters on the performance of CMOS digital logic circuits. The industry-standard MVSG (MIT Virtual Source GaN-FET Model) was used to accurately model the behavior of the n-channel and p-channel transistors, which were fabricated on the developed GaN complementary circuit platform. Furthermore, excellent matching was achieved between the experimental data of a fabricated CMOS logic inverter and the simulated compact models. Several building blocks of digital logic, namely, the logic inverter, multi-stage ring oscillator, and static random-access memory (SRAM) cell, were studied using the developed computer-aided design (CAD) framework. Device-circuit co-design was conducted to optimize circuit performance, using a variety of design parameters including transistor sizing and supply voltage scaling. The high temperature performance of the circuits, simulated based on experimentally observed trends of the devices, were projected. The results indicate that GaN CMOS technology based on our monolithically integrated platform has potential for a variety of use cases, including harsh-environment digital computation. This technique will be scaled up for more complex combinational and sequential logic building blocks, with the eventual goal of realizing a GaN CMOS microprocessor.

Further Reading:

1. N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based Complementary Logic on a Si Substrate," *IEEE Electron Device Lett.*, 2020.
2. N. Chowdhury, Q. Xie, M. Yuan, N. S. Rajput, P. Xiang, K. Cheng, H. W. Then, and T. Palacios, "First Demonstration of a Self-Aligned GaN p-FET," in *Proc. Int. Electron Device Meeting 2019*, pp. 4.6.1-4.6.4, Dec. 2019.
3. N. Chowdhury, J. Lemettinen, Q. Xie, Y. Zhang, N. S. Rajput, P. Xiang, K. Cheng, S. Suihkonen, H. W. Then, and T. Palacios, "p-channel GaN transistor based on p-GaN/AlGaN/GaN on Si," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1036-1039, Jul. 2019.

Jaeyoung Jung
jungj@mit.edu
Profile: https://mtlresume.mit.edu/profile/jaeyoung-jung