First Demonstration of GaN Vertical Power FinFETs on Engineered Substrate

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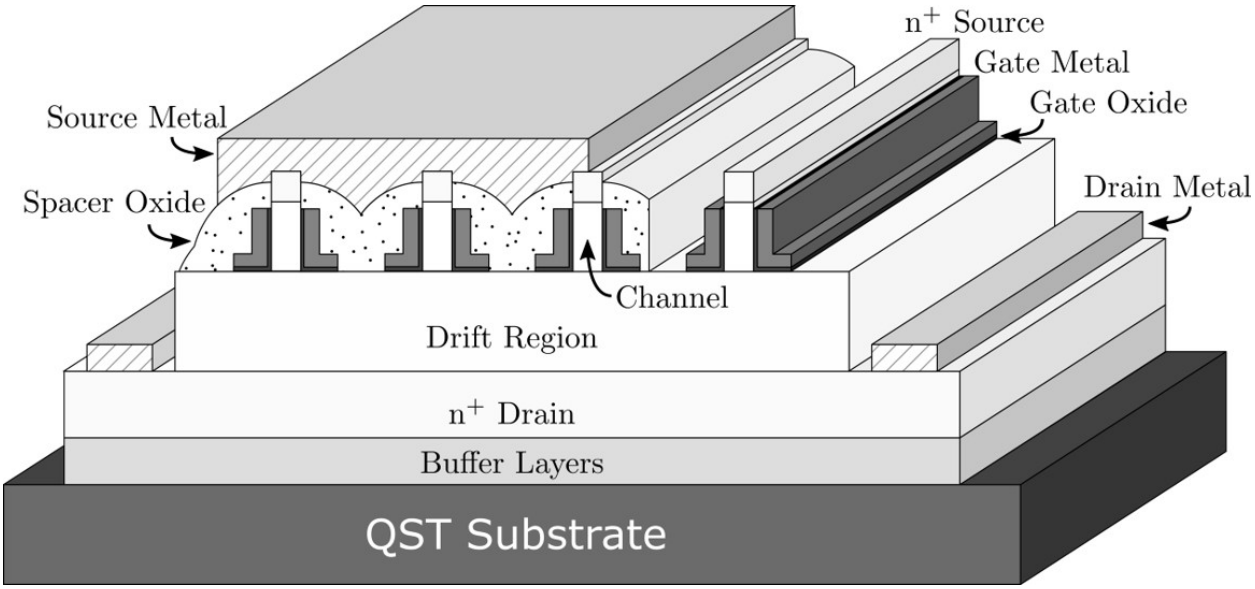
GaN vertical power FinFETs are promising high voltage switches for the next generation of high-frequency power electronics applications. Thanks to a vertical fin channel, the device offers excellent electrostatic and threshold voltage control, eliminating the need for epitaxial regrowth or p-type doping unlike other vertical GaN power transistors. Vertical GaN FinFETs with 1200 V breakdown voltage (BV), 5 A current rating and excellent switching figure of merit have been demonstrated recently on free-standing GaN substrates. Despite this promising performance, the commercialization of these devices has been limited by the high cost ($50-$100/cm^2) and small (~ 2 inch) diameter of free-standing GaN substrates. The use of GaN-on-Si wafers could reduce the substrate cost by ×1000, however the growth of the thick (~10 µm or thicker) drift layers required for kV class applications is extremely challenging on Si. Alternatively, GaN grown on engineered substrates (QST®) with a matched thermal expansion coefficient could enable low cost vertical GaN FinFETs with thick (>10 µm) drift layers and large wafer diameters (8-12 inch). In this work, we have demonstrated a quasi-vertical GaN FinFET on engineered QST® substrates for the first time.

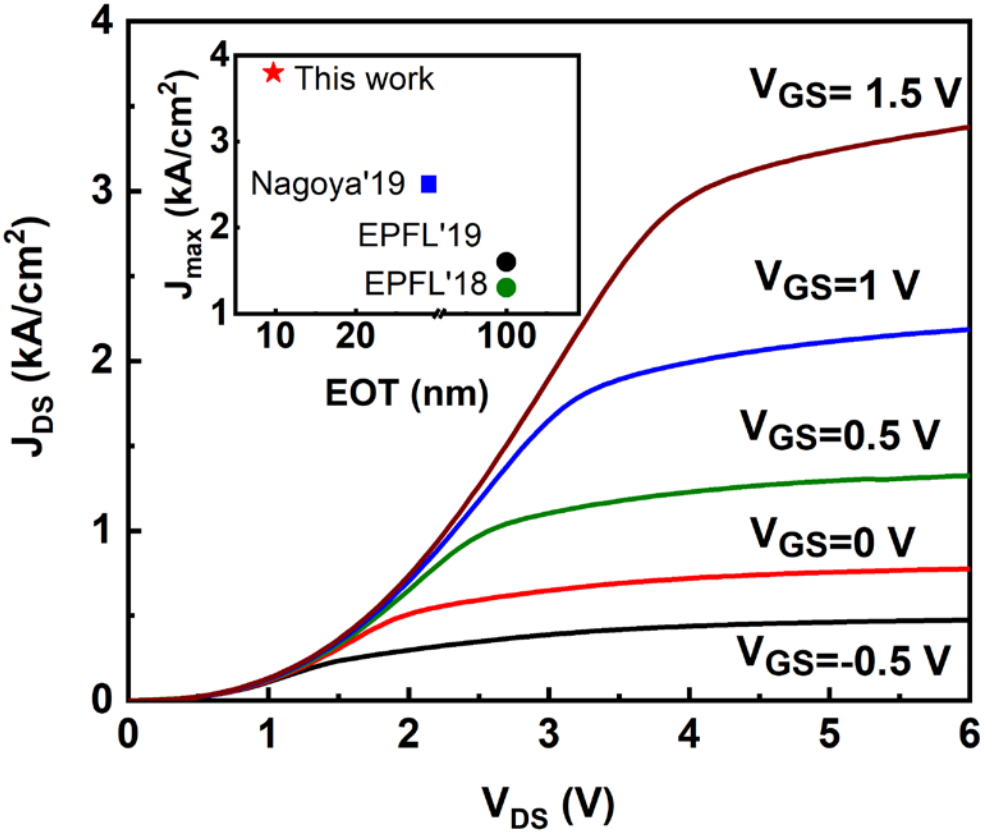
A conformal oxide-based planarization and etch-back technology was used for gate etch and source-to-gate spacer etch. The device demonstrates a current density J_{DS}=3.8 kA/cm^2 at V_{GS}= 1.5 V and V_{DS}= 4 V (Figure 2), and a maximum g_m = 2 kS/cm^2 at V_{DS}= 4 V when normalized with respect to the total device area (fin width and spacing between fins), a record for vertical and quasi-vertical MOSFETs on non-GaN substrates. The current density in each fin is higher than 30 kA/cm^2 at the same bias condition. The on-resistance is currently limited by non-ideal source contacts as is evident in the Schottky-like behavior of the drain current at low V_{DS}. The source contact resistance can be improved by either higher doping density or rapid thermal annealing of the metal stack after contact formation. The results are very promising for large wafer scale manufacturing and commercialization of vertical GaN power FinFETs.

<Figure 1 here>	<Figure 2 here>
Figure 1: Schematic diagram of the quasi vertical FinFET on QST® substrate.	Figure 2: Output characteristics of the fabricated GaN power FinFET at different gate bias. The current is normalized to total active device area. Inset shows the benchmarking of current work against the state of the art vertical GaN transistors on non-GaN substrate

Further Reading

- Y. Zhang *et al.*, 2017 IEEE International Electron Devices Meeting (IEDM), 9.2.1-9.2.4, 2017.
- C. Liu *et al., IEEE Electron Device Letters*, vol. 39, no .1, pp. 71-74, 2018.
- D.Biswas *et al.,* Semiconductor Science and Technology, 3**4**(9), (2019).


n+ Source
Gate Metal
Gate Oxide
Source Metal
Drain Metal
Spacer Oxide
Channel
Drift Region
n+ Drain
Buffer Layers
QST Substrate


This work
Nagoya'19
EPFL'19
EPFL'18
Jmax (kA/cm2)
EOT (nm)
VGS= 1.5 V
VGS=1 V
VGS=0.5 V
VGS=0 V
VGS=-0.5 V
JDS (kA/cm2)
VDS (V)