

First Demonstration of GaN CMOS Logic on Si Substrate operating at 300 C

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The power density (and form-factor) of the power electronic circuits is mostly dominated by the size of the passive energy storage components like inductors and capacitors, which depends on the switching frequency. By increasing the switching frequency of power electronic circuits, the energy storage requirement of these components can be significantly reduced, which allows for smaller components. However, the maximum operating frequency of a state-of-the-art GaN transistors, one of the promising candidates for high voltage compact switches, is typically limited by the gate inductance between the gate electrode and the driver circuit. This inductance can be significantly reduced by monolithically integrating GaN based driver circuit and with that of GaN power transistor on the same chip.

To increase the efficiency of such GaN-based ICs, a CMOS-like circuit technology is needed. Major benefits of such a technology includes zero/negligible static power dissipation, higher noise immunity and linearity. However, the lack of high-performance GaN p-FETs and the challenges of its monolithic integration with E-mode n-FET devices are major roadblocks towards achieving such a technology. This work demonstrates a new GaN-based complementary circuit platform on 6 inch Si substrate. Fig. 1(a) shows the schematic cross-section of the demonstrated GaN complementary inverter. Fig. 1(b) shows the top view of the fabricated device.

Fig. 2 (a) shows the voltage transfer characteristics (VTC) of the inverter for a V_{DD} of 5 V along with output current. The inverter shows a record voltage gain of 27 V/V for a voltage switching of 0-to-5 V. Fig. 2 (b) shows the VTC of the same inverter for $V_{DD}=3$ V exhibiting excellent inverting behavior with $V_{swing}=2.91$ V and maximum gain of ~ 15 V/V. The dynamic switching of the inverter was characterized by connecting the inverter input to a pulse generator, and the output to the high impedance port of an oscilloscope. The V_{DD} was kept at 3 V because of the high gate leakage in the p-GaN gated n-FET above that voltage. The voltage of the input pulses varied from -0.2 V to 3 V with a ramp time of 100 ns. Measured waveforms of the input and output signals are presented in Fig. 2(c)-(d). The output signal showed a voltage swing close to 0~3 V. The fall time was 1 μ s; and rise time was 20 μ s. It should be noted that these times represent an upper bound on the fall and rise times, as the measurements are limited by the very high input capacitance of the oscilloscope port (~ 350 pF).

High temperature measurement of the inverter shows a reduction in the voltage gain as shown in Fig.3(a). The maximum available voltage swing at the output is also reduced due to the rise of low-level V_{out} , which can be attributed to the reduction in ON-OFF current ratio of the p-FET at high temperature.

While there is room for significant performance improvement, this demonstration opens up a number of application domains for GaN such as integrated CMOS driver circuits, CMOS logic, logic and signal conditioning under harsh environment operation, among many others.

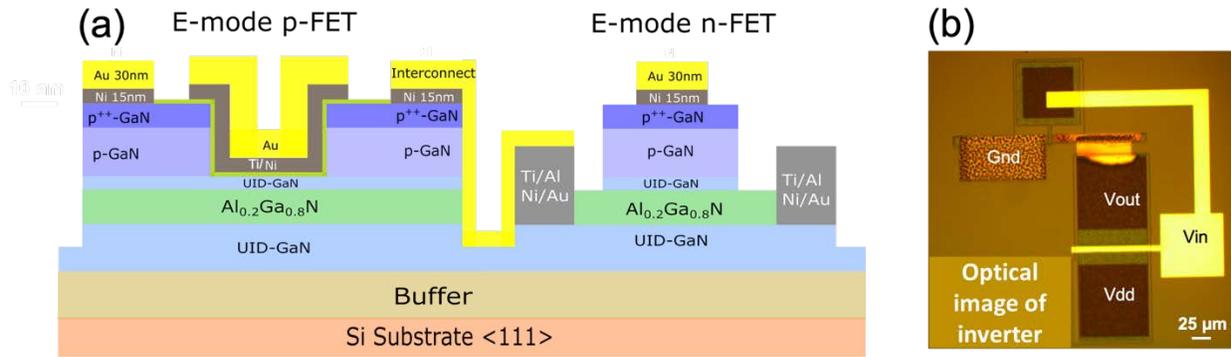


Fig. 1: (a) Schematic of the demonstrated GaN complementary circuit platform; (b) Optical image of the complementary logic inverter fabricated on this platform.

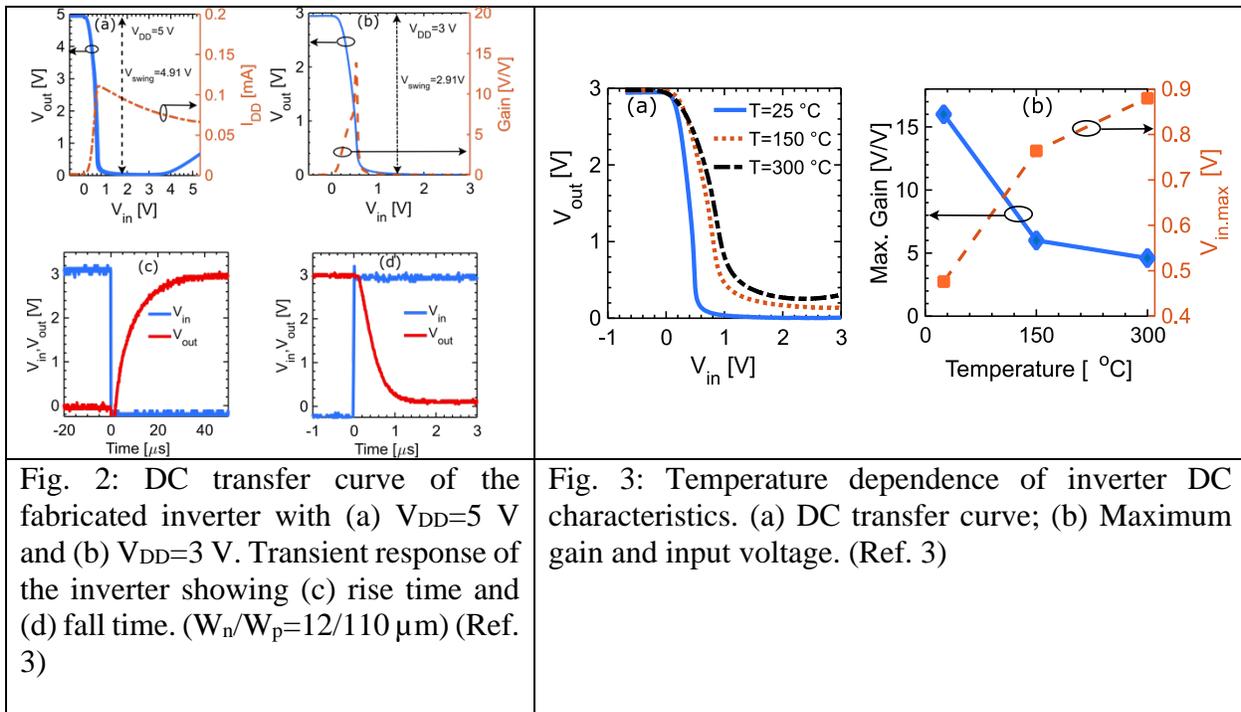


Fig. 2: DC transfer curve of the fabricated inverter with (a) $V_{DD}=5\text{ V}$ and (b) $V_{DD}=3\text{ V}$. Transient response of the inverter showing (c) rise time and (d) fall time. ($W_n/W_p=12/110\text{ }\mu\text{m}$) (Ref. 3)

Fig. 3: Temperature dependence of inverter DC characteristics. (a) DC transfer curve; (b) Maximum gain and input voltage. (Ref. 3)

Further reading:

[1] N. Chowdhury, J. Lemettinen, Q. Xie, Y. Zhang, N. S. Rajput, P. Xiang, K. Cheng, S. Suihkonen, H. W. Then, and T. Palacios, "p-Channel GaN Transistor Based on p-GaN/AlGaIn/GaN on Si," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1036-1039, Jul. 2019, DOI: 10.1109/LED.2019.2916253.

[2] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based complementary logic on a Si substrate," *IEEE Electron Device Letters* vol. 41, 2020 (DOI: 10.1109/LED.2020.2987003)