

100 nm Channel Length E-mode GaN p-FET on Si Substrate

Nadim Chowdhury, Qingyun Xie, Mengyang Yuan and Tomás Palacios

Sponsorship: Intel Corporation

GaN-CMOS-technology which could instrumental towards realizing high-power-density, high speed, low-form-factor and highly-efficient power electronic circuits, sparked a number of research into development high performance GaN p-FET. However, most of these demonstrations show normally-ON operation with ON-resistance over $1 \text{ k}\Omega\cdot\text{mm}$. GaN/AlInGaN heterostructure-based p-FET shows low ON-resistance because of higher 2-DHG density and hole mobility but with D-mode operation. GaN/AlN heterostructure based p-FET shows E-mode operation with R_{ON} of $640 \Omega\cdot\text{mm}$. However, n-FET integration with this p-FET requires regrowth.

In this work, we demonstrate a self-aligned p-FET with a GaN/Al_{0.2}Ga_{0.8}N (20 nm)/GaN heterostructure grown by metal-organic-chemical vapor deposition (MOCVD) on Si substrate. The utilization of GaN-on-Si platform offers lower cost, availability of 200-mm-diameter substrates, and potential to integrate with high performance logic and analog functionality.

While most of the GaN p-FET demonstrations so far in the literature, mainly focused on recessed gate MISFET structure, we choose to develop a self-aligned structure (see Fig. 1 for the device structure)as it offers the following advantages over recessed gate MIS p-FET.

1. Shortest possible source to the drain distance cutting down the access region.
2. Offers low on resistance because of negligible access resistance.
3. Easier gate alignment.

Our 100 nm channel length self-aligned device with recess depth of 70 nm exhibits a record ON-resistance of $400 \Omega\cdot\text{mm}$ and ON-current over 5 mA/mm with ON-OFF ratio of 6×10^5 when compared with other p-FET demonstrations based on GaN/AlGaN heterostructure (see Fig. 2 for benchmarking of our device with other p-FET demonstrated in the literature). The device shows E-mode operation with a threshold voltage of -1 V , making it a promising candidate for GaN-based complementary circuit that can be integrated on a Silicon platform. A monolithically integrated n-channel transistor with p-GaN gate is also demonstrated.

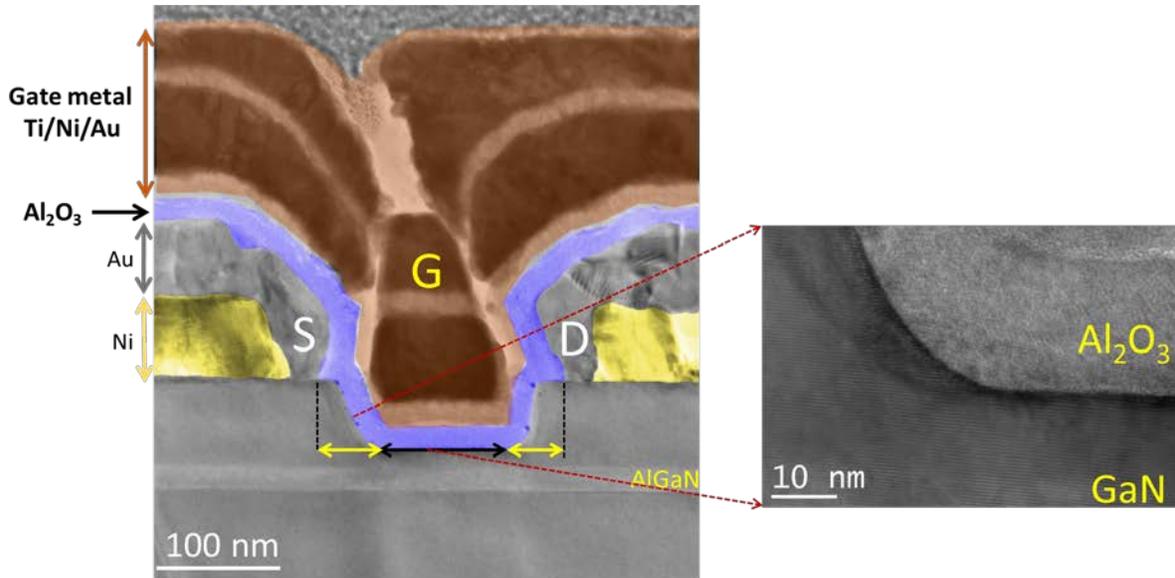


Fig 1: Transmission electron microscopy (TEM) image of the fabricated self-aligned p-FET with 100 nm channel length. Zoomed TEM image showing the smooth interface between the GaN and gate dielectric attesting to the high quality of gate recess process with low surface roughness.

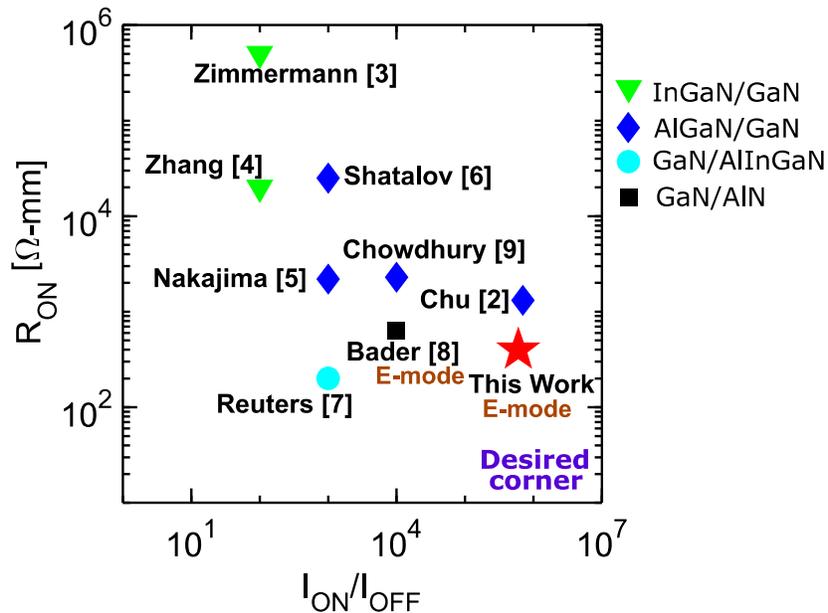


Fig. 2: Benchmarking of the reported self-aligned p-FET with other demonstrated p-FETs in the literature in terms of ON-resistance and ON-OFF ratio. It is quite evident that the reported device is closest to the desired corner exhibiting an ON-resistance of 400 Ω ·mm with excellent ON-OFF ratio of 6×10^5 . The p-FET in this work enables easy integration with on-chip n-FET without any regrowth, as illustrated in Fig. 5(a). The device is E-mode with -1 V threshold voltage. This work

shows record ON-resistance and ON-OFF ratio for any GaN-based E-mode p-FET, making it a promising candidate for GaN-based complementary logic.

Further reading:

[1] N. Chowdhury, Q. Xie, M. Yuan, N. S. Rajput, P. Xiang, K. Cheng, H. W. Then, and T. Palacios, "First Demonstration of a Self-Aligned GaN p-FET". *IEEE International Electron Devices Meeting (IEDM)*, pp. 4.6.1-4.6.4, Dec. 2019. DOI: 10.1109/IEDM19573.2019.8993569.

[2] N. Chowdhury, J. Lemettinen, Q. Xie, Y. Zhang, N. S. Rajput, P. Xiang, K. Cheng, S. Suihkonen, H. W. Then, and T. Palacios, "p-Channel GaN Transistor Based on p-GaN/AlGaN/GaN on Si," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1036-1039, Jul. 2019, DOI: 10.1109/LED.2019.2916253.